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(54) Pulse modulation power amplifier with enhanced cascade control method

(57) A controlled self-oscillating modulator (101) comprising a non-hysteresis comparator (102) for pulse modulation of a switching stage (103), and a voltage feedback loop (104) from the switching stage (103) to the comparator (102), said feedback loop securing stable oscillating conditions by means of at least two poles (105, 106).

Such a modulator provides a simple and stable configuration, obviating the need for a separate carrier frequency generator.

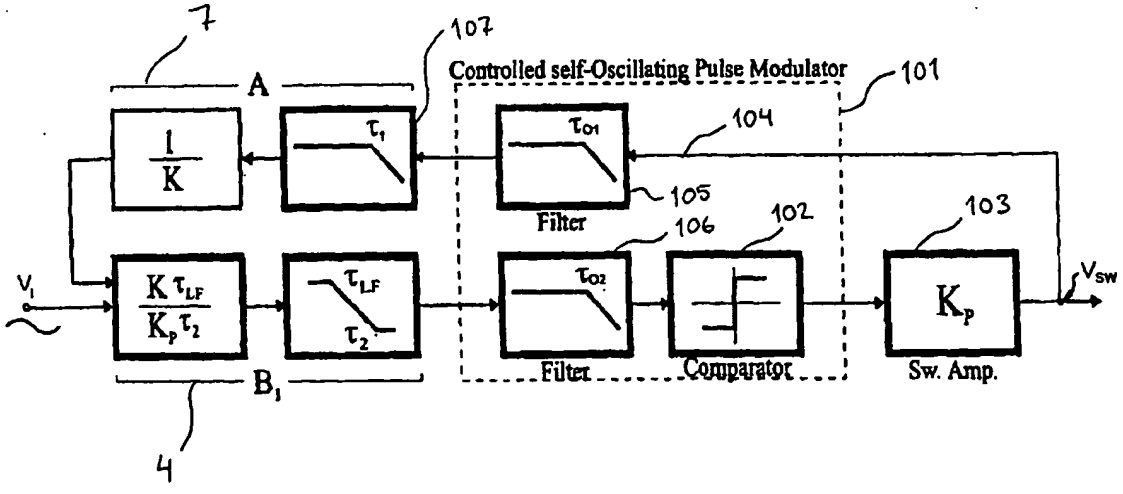

Fig. 10

EP 1 376 858 A1

Description

Technical Field

[0001] This invention relates to a power amplifier for the audio frequency range, comprising a pulse modulator, a power amplifier stage for amplifying the modulated signal, the output of which is low pass filtered in a demodulation filter for obtaining an analog output to feed to a consumer.

Background

[0002] Nearly all commercially available power amplifiers for frequencies in the above range are of the linear analog type: class A, AB, and B. Since the output transistors of such amplifiers operate in the linear region, they have a low efficiency and dissipate a considerable amount of heat. The basic pulse modulation ("digital") switching class D power amplifier method in theory provides a much higher efficiency, which lowers the amplifier volume and heat development. Despite this efficiency advantage, prior art in the field has not provided solutions with an acceptable audio quality, that could make them generally useful and direct replacements for analog amplifiers. Accordingly, the use of digital power amplification has been limited to applications where the demands for output quality are low. The reasons for this will be presented in the following, when the general prior art principles are discussed.

Prior Art

[0003] There is a fundamental requirement for efficient control systems to eliminate errors generated in the various blocks of the digital switching power amplifier. In the basic digital power amplifier the input signal is modulated into a pulse modulated signal. A switching power stage performs amplification of the signal, and a low pass filter regenerates the modulated but now amplified signal. The basic method form the basis for a range of prior art arrangements. However, there are numerous non-ideal features with this method :

- Any modulator errors are fed directly to the load.
- Any power stage errors are fed directly to the load.
- There is no rejection of power supply perturbations. Since the power stage output is largely proportional to the supply voltage, any supply ripple will intermodulate with the audio signal.
- The post filter errors will introduce further distortion, since magnetic core materials are not ideal.
- The total output impedance is high, especially at high frequencies, due to the filter.
- The sensitivity to load variations is high due to the passive post filter. Accordingly, changes in load impedance will distort the frequency response of the amplifier.
- The sensitivity to temperature drift, component tolerances, and aging effects is high. The non-controlled digital switching amplifier is therefore not robust and reliable.

[0004] Compensation for these major problems areas is absolutely vital, if very high fidelity is to be obtained. Prior art methods are based on two different control methods, characterized by having a single feedback loop.

[0005] One basic principle is to feed back the amplifier output. However, the poles of the low pass filter cause a large phase shift which puts strong restrictions on loop design. Consequently, reasonable loop bandwidths requires high switching frequencies. This causes several problems, such as lower efficiency, and poor performance due to the first two errors mentioned above.

[0006] Another basic principle of feedback in prior art, is single loop feedback before the filter network, whereby the phase lag of the post filter is avoided. However, the high frequency content at the power stage output makes the feedback source potentially very noisy. Furthermore, a number of the above errors are not (or only partially) compensated .

[0007] The fundamental problem of both methods are the conflicting desires for a low carrier frequency, high gain-bandwidth product and good stability characteristics in all situations. A further problem with prior art arrangements is the apparent complexity of the system, partially caused by inefficient control.

[0008] The following publications are relevant as background material and illustration of the methods and the problematic issues of three prior art arrangements:

[1] Suzuki, T. : Pulse Width Modulated Signal Amplifier. US Patent no. 4021745 (1977)
[2] Yokoyama, K. : Pulse-Width Modulation Circuit. US Patent no. 4531096 (1986)
[3] Attwood, B.E. : Design Parameters Important for the Optimization of Very High-Fidelity PWM (Class D) Audio Amplifiers , Journal of the AES, Nov. 1983. p. 842-853.

[4] Taylor, W.E. : Digital Audio Amplifier . US Patent. No. 4724396 (1988).
[5] Hancook, J. : A class D Amplifier Using MosFET's with Reduced MinorityCarrier Lifetime , 89th Convention of the AES. Los Angeles. CA. September 21-25. 1991.
[6] Solomon, E.E : Digital Power Amplifier. US Patent No. 5126684 (1992).
[7] McCorkle, D.P. Class D amplifier. European Patent. Publ. No. 557032A2 (1993).
[8] Nakajima, Y. Pulse-Width Modulation amplifier. European Patent. Publ. No.503571A1 (1993).
[9] Leigh, S.P et al. Distortion analysis and reduction in a completely digital PWM class D power amplifier, International Journal of Modeling & Simulation, Vol. 14, No. 2, 1994.

OBJECTIVES

[0009] According to the above stated problems that exist with prior art arrangements, the primary objective of the present invention is to provide a pulse modulation amplifier which can deliver very high power outputs, and still provide ultra low distortion (less than 0.01%) and noise (less than 100μV RMS), and yet a very high efficiency (90-95%) and low idle losses.

[0010] Another objective of the invention is to maintain low complexity by avoiding the use of advanced but complex and hence potentially unreliable circuitry, and also to eliminate the requirement for tuning in production.

[0011] Another important objective of the invention is to eliminate the need for a stabilized supply, meaning that a simple non-regulated bridge rectifier with a stabilizing capacitor is sufficient. In this way, a minimal complexity and maximal efficiency is secured from the mains input to the amplifier output terminals.

[0012] The final objective of the invention is to obtain minimal sensitivity to load variations, and furthermore to provide robustness and reliability.

SUMMARY OF THE INVENTION

[0013] The above objectives are obtained with the present invention. In the first preferred embodiment, an amplifier according to the invention is particular in that negative feedback is introduced from the switching power stage output to one or several loops feeding into one or several pre-amplifier stages preceding the modulator. This offers a range of advantages that are new to the art, in terms of performance and stability control. A further embodiment of the invention is particular in that the local feedback has a enhanced cascaded structure with a single feedback path, that comprises a filter with a phase characteristic such that a pole in the demodulation filter is compensated.

[0014] Another embodiment of the invention is particular in that further feedback is established from the output of the demodulation filter to one or several pre-amplifier stages, so that the pulse modulation ("digital") switching power amplifier circuit elements are enclosed by an enhanced cascade structure of feedback loops, providing further improved performance and stability control.

[0015] A further embodiment of the invention is particular in that the pulse modulator is a controlled self-oscillating modulator comprising a non-hysteresis comparator for pulse modulation, and a higher order oscillating loop realized by means of two poles, preferably a pole in the first (local) forward path and feedback path. This provides en extremely simple and stable configuration, obviating the need for a separate carrier frequency generator.

[0016] A further embodiment of the invention is particular in that the pulse modulator is a carrier based modulator. This means that well-known design techniques for carrier based modulators may be used in the configuration according to the invention.

[0017] A further advantageous embodiment of the invention when carrier based modulation is used, is particular in that a notch filter is provided in the single feedback path block between the amplifier and the loops. Thereby it is possible to simplify the filtering out of the carrier frequency influences on the system performance in carrier based systems. A similar result is obtained in a further advantageous embodiment of the invention which is particular in that a structure creating a high frequency pole is provided in the feedback path block.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The invention will be further described with reference to the drawings, in which,

Fig. 1 shows the principle in prior art conventional pulse modulation ("digital") switching power amplifiers

Fig. 2 shows a prior art method with single loop feedback based on the overall amplifier output as the feedback source

Fig. 3 shows a prior art single loop feedback with power stage output as the feedback source

Fig. 4 shows the a general block diagram of a first embodiment of the present invention, a digital switching amplifier improved by an Multivariable Enhanced Cascade Controller (MECC) based on single feedback from the switching power stage output.

Fig. 5 shows a general block diagram of a second embodiment of the present invention,

Fig. 6a and 6b exemplify general recursive loop synthesis methods for the first (Fig. 6a) and second (Fig. 6b) embodiments of the invention.

Fig. 7 shows a detail of a preferred embodiment of single feedback MECC.

Fig. 8 shows a detail of a preferred example of the second embodiment of the invention, the dual feedback Multivariable Enhanced Cascade Controller (MECC).

Fig. 9a and 9b show the loop characteristics for the two preferred examples of the first two embodiments of the present invention, shown in Fig. 7 and Fig. 8.

Fig. 10 illustrates the third embodiment of the present invention, the controlled self-oscillating pulse modulator characterized by a non-hysteresis comparator and additional poles in the first local loop to secure self-oscillating conditions

Fig. 11 shows essential signals of the third embodiment of the invention, the controlled oscillating pulse modulator.

Fig. 12 illustrates the principle of a fourth embodiment of the invention, an alternative three-level pulse width modulator for implementation with a 4 transistor bridge power stage. The signals are from top to bottom : Modulating signals, normalized voltage on each phase in a bridge power stage (A,B), and finally both the normalized differential and common mode output signals (A-B and A+B) . The difference signal is fed to the load.

Fig. 13 illustrates the spectral characteristics of the alternative three-level modulator. The output amplitude spectrum is shown 0dB and -60dB relative output levels.

Fig. 14 (a)-(c) illustrate various performance specifications for an implemented example embodiment of the invention with a 250W maximal power handling capability. Fig. 13 (a) shows power efficiency. At 250kHz switching frequency the efficiency approaches 92%, and with 50kHz switching frequency the efficiency approaches 96%.

Fig. 14 (b) shows the very low measured Total harmonic distortion + Noise (THD+N) vs. output power at 100Hz, 1KHz and 10KHz (top curve).

Fig. 14c (c) shows the measured amplifier noise. The noise floor at -150dB corresponds to an RMS noise level of only 70μV.

DETAILED DESCRIPTION

[0019] The basic "digital" power amplifier is shown in Fig. 1. The input signal is modulated (11) into a pulse modulated signal. A switching power stage (12) performs amplification of the modulated signal, and a low pass filter (13) regenerates the audio waveform.

[0020] A first category of prior art control principle is shown in Fig. 2. This displays the basic problems: that a reasonable gain- bandwidth product requires very high switching frequencies due to post filter phase lag and the lack of local correction schemes. Reasonable gain-bandwidth product at all frequencies within the amplifier bandwidth is impossible to obtain.

[0021] Fig. 3 shows a second category of prior art control principles which displays the following basic problems: noisy feedback source, no post filter error correction, load sensitivity and limited loop gain-bandwidth product caused by single loop control.

[0022] Fig. 4 illustrates the first embodiment of the invention. The basic pulse modulation ("digital") switching power amplifier circuit elements are enclosed by an enhanced cascade (or nested) structure of feedback loops. This first embodiment is termed a (single feedback) Multivariable Enhanced Cascade Controlled (MECC) digital power amplifier. The control structure is characterized first by having a single feedback source and second by a single feedback path A (7) having a lowpass characteristic. The control structure is simple in implementation since it consists of a single

feedback path A and a set of forward path blocks B_i. Using preferred loop design procedures, each loop has a very stable 1st order characteristic and the forward path blocks are preferably simple. MECC offers a range of advantages that are new to the art:

- A higher order control system combined with a high level of stability and robustness, since each loop considered individually is very stable.
- The enhanced cascade control method provides hitherto unknown freedom in loop design and optimization possibilities. Thus, the equivalent loop gain bandwidth at any frequency can as such be increased infinitely relative to single loop systems without compromising stability.
- The lowpass characteristic of the feedback path provides a closed loop zero-pole lead characteristic that can be designed to cancel one of the filter poles. The result is a much improved system for global feedback.
- Each loop individually reduces the sensitivity to power stage errors and improves system performance (distortion, noise...) by a factor corresponding to the loop gain. MECC provides an equivalent feedback corresponding to the product of contributions of each loop.
- Successive improvement by multiple loops is more efficient than in a one loop realization.
- Frequencies of unity loop gain in each loop can be reduced compared to single loop system, while still providing improved performance. Thus, the switching frequency can be reduced.
- MECC has low requirements for dynamic range of the individual compensator blocks A and B_i. Using preferred design procedures, the signal levels throughout the control system will have a level similar to the input signal.

[0023] The second embodiment of the invention involves the extension of the first embodiment to a dual feedback Multivariable Enhanced Cascade Control (MECC)structure, were the two cascades are closely connected. A general block diagram is illustrated in Fig. 5. The system relies on the zero-pole lead characteristic caused by the single lowpass feedback path of the local enhanced cascade. Dual feedback MECC provides further improvements to the system. The system bandwidth is increased beyond the demodulation filter bandwidth limit. This minimizes phase and amplitude distortion within the audio band. Furthermore, the transient response is improved. Post filter errors are corrected, meaning that the requirements for filter inductor linearity is low. Furthermore, the output impedance is reduced considerably, and so is the sensitivity to load variations.

[0024] A third embodiment of the invention is a forced self-oscillating pulse width modulator, characterized by first a non-hysteresis comparator as a modulator and secondly by a higher order oscillating loop realized with both forward path B1 and feedback path A to determine self-oscillating conditions.

[0025] A fourth embodiment of the invention is an alternative carrier based three-level pulse width modulator with attractive characteristics in combination with MECC.

[0026] Further embodiments of the invention include :

- Means for obtaining improved elimination of noise from the noisy feedback by using a notch filter and high frequency poles in the local feedback or alternatively forward path. This improves distortion when carrier based pulse width modulation is used.
- Means for compensating for large scale power supply regulation, in order to obtain improved stability and efficiency improvements at all output levels. This is relevant with carrier based modulation, where the gain of modulator and power stage is dependent on the power supply rail level, meaning that the power supply perturbation may influence stability unless such precautions are taken.

DESCRIPTION OF THE FIRST EMBODIMENT

[0027] The enhanced cascade control method new to the art relies on the fact that the modulator and amplifier can be represented by a constant gain K_p over a wide bandwidth. One general recursive approach to design the local cascade is illustrated in Fig. 6a. The feedback path has a lowpass characteristic:

$$A(s) = \frac{1}{K}\frac{1}{\tau_1 s + 1} \tag{1}$$

[0028] The lowpass characteristic of the feedback path is beneficial in several aspects. It causes a closed loop zero-pole phase *lead* characteristic which can be very useful for realizing a cancellation of one of the poles of the demodulation filter. Furthermore, the pole causes an important filtering of the high frequency switching noise from the power stage output, which is essential when carrier based modulation methods are used (the fourth embodiment of the invention). In this simple examplary embodiment the initial forward block is a simple gain, with a gain that leads to a constant open loop and closed loop gain of K in the frequency band of interest:

$$B_1(s) = \frac{K}{K_P}\frac{\tau_1}{\tau_2} \tag{2}$$

[0029] Whereas the i'th block has a pole-zero characteristic to compensate for the zero-pole characteristic of the preceding loop:

$$B_i(s) = \frac{\tau_1}{\tau_2}\frac{\tau_2 s + 1}{\tau_1 s + 1} \tag{3}$$

[0030] By this realization the open loop gain of the single loop configuration can be written by the following 1. order expression:

$$\begin{aligned} HL_{1,ol}(s) &= K_P A(s) B(s) \\ &= K_P \frac{1}{K}\frac{1}{\tau_1 s + 1}\frac{K}{K_P}\frac{\tau_1}{\tau_2} \\ &= \frac{1}{\tau_1 s + 1}\frac{\tau_1}{\tau_2} \end{aligned} \tag{4}$$

[0031] It is easy to show that for all loops:

$$HL_{i,ol}(s) \equiv HL_{1,ol}(s) = \frac{\tau_1}{\tau_2}\frac{1}{\tau_1 s + 1} \tag{51}$$

[0032] The closed-loop transfer function can be approximated to:

$$HL_{i,cl}(s) \cong K\frac{\tau_1 s + 1}{\tau_2 s + 1} \tag{6}$$

[0033] By this specified simple loop synthesis procedure, each loop will exhibit *identical* and stable 1st order behaviour as illustrated in Fig. 6a.

[0034] Numerous alternative approaches to loop synthesis can be devised. The recursive design procedure specified above provides a frequency independent loop gain at all frequencies within the target bandwidth, irrespective of the number of cascaded loops and the loop unity gain frequency. Instead of a constant loop gain, each loop can realize e.g. an integrator. Alternatively, each loop can be designed using two pole compensation. Both methods lead to a considerably higher but frequency dependent loop gain within the frequency band of interest.

[0035] Alternative variants of single feedback MECC power amplifier include the use of alternative different feedback paths A, which are optimized in respect to noise attenuation , which is essential in systems where carrier based modulation is used. If HF components related to the switching frequency were to reach the modulator, it would be impossible to obtain a pulse width according to the instantaneous amplitude of the audio signal. By introduction of a notch filter, the first critical component and intermodulation components can be eliminated. The specific placement of the notch

filter in the feedback path effectively eliminates the switching fundamental in *all* loops. By further addition of a high frequency pole in block A, a 2nd order attenuation characteristic of the higher order harmonics of the switching frequency in the feedback path is realized, and the noise attenuation is thereby further improved. A further advantage of placing the noise attenuating circuitry in the feedback path is, that it will only have a *local* effect for each loop, if the unity loop gain frequency and switching frequency are properly chosen. The noise elimination circuitry operates well above unity loop gain, and does therefore not influence the closed loop behavior of any of the loops.

DESCRIPTION OF THE SECOND PREFERRED EMBODIMENT

[0036] The second embodiment of the invention involves the extension of the first embodiment to a dual feedback Multivariable Enhanced Cascade Control (MECC)structure, were the two cascades are closely connected. A general block diagram is illustrated in Fig. 5. The system relies on the zero-pole lead characteristic caused by the single lowpass feedback path of the local enhanced cascade. Due to the use of two feedback sources, this embodiment is termed Dual feedback Multivariable Enhanced Cascade Control. The second cascade has the same special characteristics as the first cascade with only one single feedback path C and a set of forward path blocks D_i. One preferred approach of dual feedback MECC design is based on the local enhanced cascade in Fig. 6a and illustrated in Fig. 6b. The main reconstruction filter *F(s)* is assumed to be 2. order. The feedback path has a constant gain characteristic:

$$C(s) = \frac{1}{K} \tag{7}$$

[0037] The initial block forward block D_1 is a simple gain block with a gain in the frequency band of interest :

$$D(s) = \frac{\tau_1}{\tau_3} \tag{8}$$

[0038] Whereas the i'th forward block has a pole-zero characteristic :

$$D_i(s) = \frac{\tau_1}{\tau_3}\frac{\tau_3 s + 1}{\tau_1 s + 1} \tag{9}$$

[0039] By this simple recursive design procedure, each loop will exhibit identical behavior, which is illustrated by both the open loop $HG_{I,OL}(s)$ and closed loop characteristics $HG_{I,CL}(s)$ in Fig. 6b:

$$HG_{i,ol}(s) \equiv HG_{1.ol}(s) = \frac{\tau_1}{\tau_3}\frac{1}{(\tau_1 s + 1)(\tau_2 s + 1)} \tag{10}$$

[0040] The closed-loop transfer function can be approximated to :

$$HG_{i,cl}(s) \cong \frac{K}{(\tau_3 s + 1)(\tau_2 s + 1)} \tag{11}$$

[0041] It should be emphasized, that the given design approach is mainly illustrative, and that there are numerous possible extensions which will be apparent to the skilled person, e.g. a first order characteristic in each loop to improve correction for errors at lower frequencies.

[0042] To maximize the robustness of the dual feedback MECC Digital power amplifier, the number of global loops should be minimized and preferably only one global loop should be used. Tuning towards the desired distortion and noise characteristics should be carried out by adjusting the number of local loops, since the dominating errors are introduced in the switching power stage block, and should therefore be corrected locally.

[0043] A fundamental advantage of the powerful Multivariable Enhanced Cascade Control method in both embodiments is, that design of modulator, power stage, post filter and power supply can be relaxed considerably without compromising audio performance. These fundamental elements can be implemented with simple standard components and thereby have a low cost and complexity.

[0044] The control method comprising first and embodiment of this invention functions independently of the pulse

modulator and power stage realization. The only requirement for theses two blocks is that they realize an amplification of the analog modulator reference input over a frequency range that is wider that the desired bandwidth. Thus, the modulation may be single sided or double sided, two level or multilevel pulse width modulation, or even alternative modulation schemes such as Sigma-Delta modulation.

THE THIRD EMBODIMENT OF THE INVENTION

[0045] A further preferred embodiment regarding modulator implementation for the MECC digital power amplifier is a Controlled self-Oscillating Pulse Modulator, new to the art. An example of an embodiment realizing this method is shown in Fig. 10. The preferred method is characterized by having a non-hysteresis comparator as a modulator and by modifying the first local loop to a have higher order characteristic, by an additional pole in both forward path block B_1 and feedback path A. This secures controlled and stable self-oscillating conditions. The desired pulse modulation effect is then obtained by superposing the oscillating signal with the signal input (V_i) . Fig. 11 shows an example of the signal characteristics at the reference point for the modulator where the oscillating signal is superposed with the input signal. Furthermore, the pulse modulating effect is shown.

[0046] Advantages of the above described Controlled self-Oscillating Pulse Modulator over constant frequency carrier based methods are several. First, the modulator is extremely simple to implement since no carrier generator is needed. Secondly, the bandwidth of the unity gain frequency of the first local loop is the oscillation frequency leading to wide bandwidth control even with modest switching frequencies. Third, power supply rail no longer determines the equivalent gain of the modulator/power stage meaning that large scale power supply perturbation is automatically cancelled, and does no longer influence stability in other loops in the enhanced cascade structure. The unity gain frequency of the local loop is inherently determined by the frequency of positive feedback, i.e. the control loop bandwidth is considerably wider than in traditional carrier based systems, where a rule of thumb is a factor of three between unity gain frequency and carrier frequency.

OTHER EMBODIMENTS

[0047] Other embodiments of the of invention include the use of pulse width modulation, preferably with three discrete amplitude levels. To aid in this understanding this alternative embodiment regarding modulator implementation, Fig. 12 illustrates the essential time domain waveforms and Fig. 13 the frequency domain spectral amplitude characteristics. From Fig. 12 it is obvious that by using three-level PWM the effective sampling frequency is doubled since there are two samples pr. switch cycle. This is obtained without increasing the power losses, since each transistor operates at a rate equal to the switching frequency. Accordingly, three-level PWM allows the loop bandwidths to be increased or alternatively the switching frequency to be decreased.

[0048] A further embodiment of the invention relates to the case where MECC is combined with constant frequency carrier based modulation, and is characterized by the design change described hereinafter. Improved means to compensate for any large scale variations of the power supply voltage is obtained by intelligent automatic gain adjustments in the first local loop. The equivalent gain of the modulator and power stage, K_p, is largely proportional to the power supply voltage. Accordingly, the gain of B_1 should be regulated inversely proportional to the supply voltage variation:

$$B_1(K_P) = \frac{K}{K_P}\frac{\tau_1}{\tau_2} \tag{12}$$

[0049] This design change will have a further stabilizing effect on the digital power amplifier based on MECC since the characteristics of the first loop will be independent power supply perturbations. Large perturbations of the power supply voltage will not influence stability. The adaptive adjustment of the power supply allows an intelligent control of the power rail voltage e.g. controlled by the volume control without compromising stability. This can be utilized to secure optimal efficiency at all output levels.

[0050] Further embodiments include additional secondary filtering circuitry on the amplifier output for further elimination of switching components, and the addition of an input filter to shape the overall amplifier response in frequency and time,

EXAMPLES OF THE FIRST AND SECOND EMBODIMENT

[0051] Fig. 7a and 7b show more specific double loop examples of both the single and dual feedback MECC embodiments. The design procedure of each loop is given in Fig. 9a and 9b respectively. Compared with the general design procedure, the LF performance has been optimized such that the equivalent loop gain in both loops is signifi-

cantly increased at lower frequencies compared to the general approach. Table 1 gives example parameter values relative to the amplifier bandwidth.

Table 1

Parameter	Frequency (rel. to bandwidth)
$1/\tau_1$,	2
$1/\tau_2$	10
$1/\tau_{LF}$	1/5

[0052] The enhanced cascade provides a significant improvement over a the single loop approaches known in the art, with only a marginal increase in system complexity in terms of the added forward block B_2. Provided that the reconstruction filter is reasonably linear, the local feedback MECC embodiment can realize high end specifications. Further improvement may be realized by adding blocks equal to B_2. Alternative use of this first embodiment of the invention is to drive loudspeakers directly without reconstruction filter.

[0053] Fig. 7b provides an example of an embodiment of dual feedback Multivariable Enhanced Cascade Control (MECC) with one local and one global loop, both closely connected. Compared to the general design procedure specified in Fig. 6 both loops have been LF optimized to significantly increase the loop gain in both loops at lower frequencies. Table 2 gives examples of parameter values relative to the amplifier bandwidth.

Table 2

Parameter	Frequency (rel. to bandwidth)
$1/\tau_1$	2
$1/\tau_2$	10
$1/\tau_3$	4
$1/\tau_{LF}$	1/5

[0054] In order to clarify the significant advantages of the dual feedback MECC digital power amplifier over prior art, the embodiment in Fig. 8 has been implemented in two higher power examples, one to cover the full audio bandwidth of 20kHz utilizing a 250kHz switching frequency, and one example covering a reduced bandwidth of 4kHz, utilizing a 50kHz switching frequency.

[0055] It should be emphasized that the chosen parameters are only illustrative, and that the MECC digital power amplifier is well performing on a much wider range of output powers and bandwidths. Figs. 14 (a) - (c) illustrate various key specifications for the given example, and the results obtained are summarized in Table 3. If further improvements are desired, one preferred approach is to use a double local loop by simple addition of a B forward block.

Table 3

Specification	Measurement
Max. power	250W
Bandwidth	20kHz / 4kHz
THD+N (1KHz, 1W)	<0.01%
THD+N (20Hz-20KHz)	<0.05%
Intermodulation distortion (IMD)	<0.01%
Idle noise (RMS) within bandwidth	70μV
Dynamic range	115dB
Power Stage Efficiency (250kHz / 50 kHz switching frequency)	92% / 96%

[0056] In general no prior art approach yields a comparable combination of fidelity, efficiency, and low complexity.

[0057] A pulse modulation power amplifier for the audio frequency range, comprising a pulse modulator, a power

amplifier stage for amplifying the modulated signal, the output of which is low pass filtered in a demodulation filter for obtaining an analog output to feed to a consumer,
characterised in that negative feedback is introduced from the power amplifier stage output to one or several loops feeding into one or several pre-amplifier stages preceding the modulator.

[0058] A power amplifier according to claim 1,
characterised in that a further feedback loop is established from the output of the demodulation filter and to the one or several pre-amplifier stages.

[0059] A power amplifier according to claim 1 or 2,
characterised in that the feedback configuration is a multi-loop configuration, at least one of the loops being constituted of a signal from the switched amplifier stage injected into the chain of preamplifier stages, and at least one other loop being a global feedback from the filtered output to the input of the amplifier.

[0060] A power amplifier according to claim 3,
characterised in that at least one feedback loop from the switching power stage output comprises a filter with a phase characteristic such that a pole in the demodulation filter is compensated.

[0061] A power amplifier according to claim 1,
characterised in that a single feedback path block (A) is used to feedback the preamplifier chain,is used and that each loop approaches stable first order characteristics.

[0062] A power amplifier according to claim 2,
characterised in that a single feedback path block (C) is used to the preamplifier chain, and that each loop approaches stable first order characteristics.

[0063] A power amplifier according to any of the preceding claims, **characterised in** that the pulse modulator is a controlled self-oscillating modulator comprising a non-hysteresis comparator for pulse modulation, and a higher order oscillating loop realized by means of two poles, preferably a pole in the forward path (B) and a pole in the feedback path (A).

[0064] A power amplifier according to any of the preceding claims, **characterised in** that the pulse modulator is a carrier based pulse modulator.

[0065] A power amplifier according to claim 7,
characterised in that a notch filter is provided in the feedback path block (A) between the amplifier and the loops.

[0066] A power amplifier according to claim 8,
characterised in that a structure creating a high frequency pole is provided in the feedback path block (A).

[0067] A power amplifier according to claim 1 and 2,
characterised in that additional secondary filtering circuitry is added at the amplifier output for further elimination of switching components.

[0068] A power amplifier according to claim 1 and 2,
characterised in that an input filter is added to shape the overall amplifier response in frequency and time.

[0069] A power amplifier according to claim 1 and 2, **characterised in** that improved means to compensate for any large scale variations of the power supply voltage is obtained by adaptive gain adjustments in the first local loop.

Claims

1. A controlled self-oscillating modulator (101) comprising a non-hysteresis comparator (102) for pulse modulation of a switching stage (103), and a voltage feedback loop (104) from the switching stage (103) to the comparator (102), said feedback loop securing stable oscillating conditions by means of at least two poles (105, 106).

2. A controlled self-oscillating modulator according to claim 1, wherein said feedback loop (104) comprises a feedback path (7) providing a feedback signal to a forward path (4), said feedback signal being superposed with a reference signal (V_i) in the forward path, said feedback path (7) comprising at least one pole (105), and said forward path (4) comprising at least one pole (106).

3. A controlled self-oscillating modulator according to claim 2, wherein said feedback path (7) comprises at least two poles (105, 107), one of said poles (107) compensating a pole in a demodulation filter (6) connected to the switching stage.

4. A pulse modulation power amplifier for the audio frequency range, comprising a controlled self-oscillating modulator (101) according to claim 1 - 4, and a switching power stage (103; 5) for amplifying the modulated signal, the output of which is low pass filtered in a demodulation filter (6) for obtaining an analogue output to feed to a consumer.

5. A pulse modulation power amplifier according to claim 4, wherein said feedback path (7) is connected to at least two pre-amplifier stages (3, 4) preceding the modulator, to form at least two local feedback loops.

6. A power amplifier according to claim 5, wherein a single feedback path is used for all local feedback loops.

7. A power amplifier according to claims 5 or 6, wherein each local feedback loop has stable first order open loop characteristics.

8. A power amplifier according to claim 4 - 7, further comprising a negative feedback from the output of the demodulation filter (6) to at least one feedback path (8), connected to one or several pre-amplifier stages (1, 2), to form one or several global feedback loops.

9. A power amplifier according to claim 8, wherein the feedback from the switching stage (5) is connected to a first group of pre-amplifier stages (3, 4), and the feedback from the demodulation filter (6) is connected to a second group of one or several pre-amplifier stages (1, 2), preceding said first group.

10. A power amplifier according to claims 8 or 9, wherein a single feedback path is used for all global feedback loops.

11. A power amplifier according to claims 8 - 10, wherein each global feedback loop has stable first order open loop characteristics.

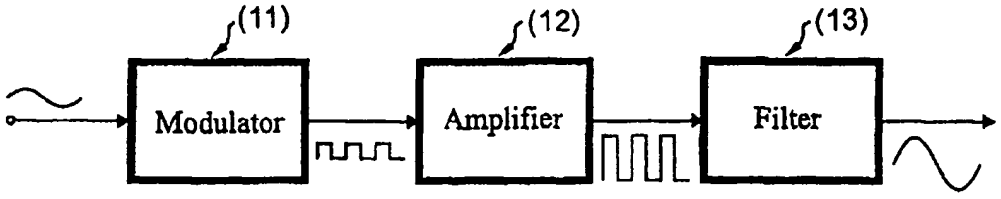

Fig. 1 (Prior art)

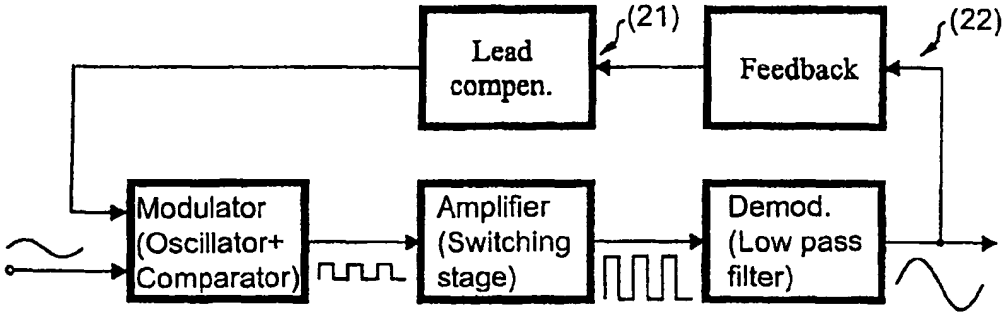

Fig. 2 (Prior art)

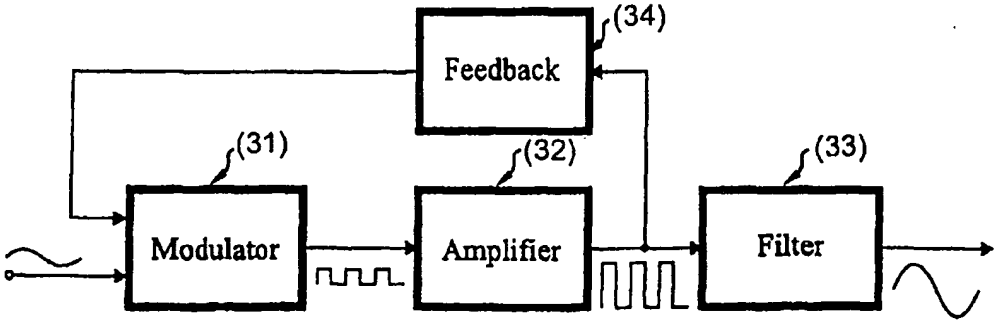

Fig. 3 (Prior art)

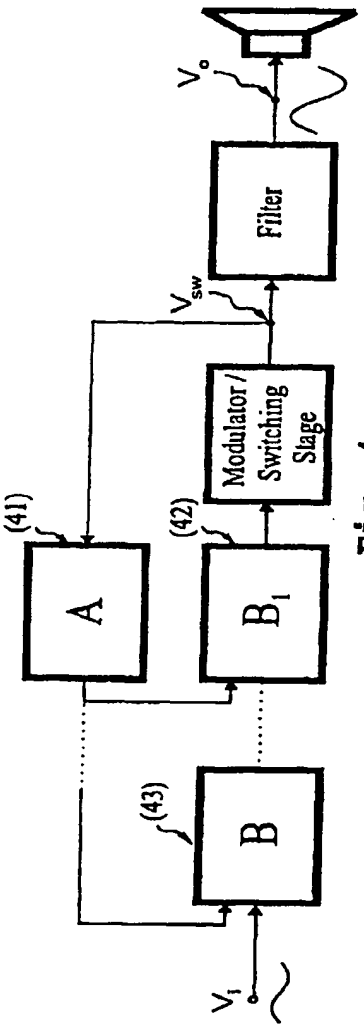
V_o
Filter
V_{sw}
Modulator / Switching Stage
(41)
(42)
(43)
A
B_1
B
V_i

Fig. 4

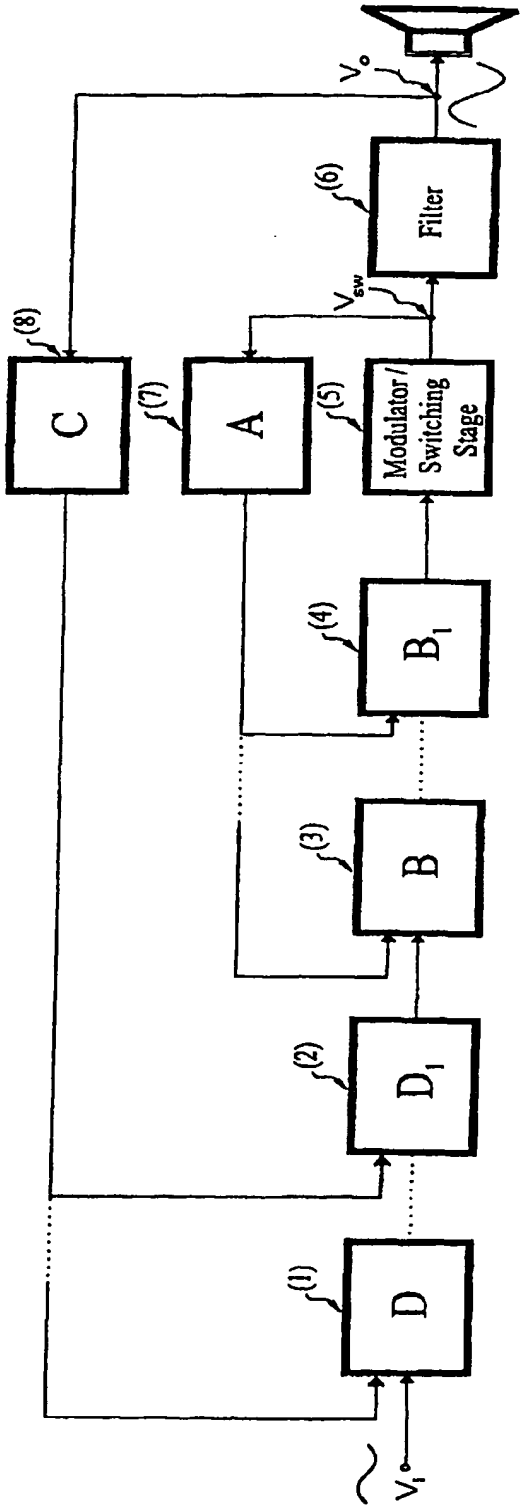
V_o
(6)
Filter
V_{sw}
(8)
(7)
(5)
C
A
Modulator / Switching Stage
(4)
B_1
(3)
B
(2)
D_1
(1)
D
V_i

Fig. 5

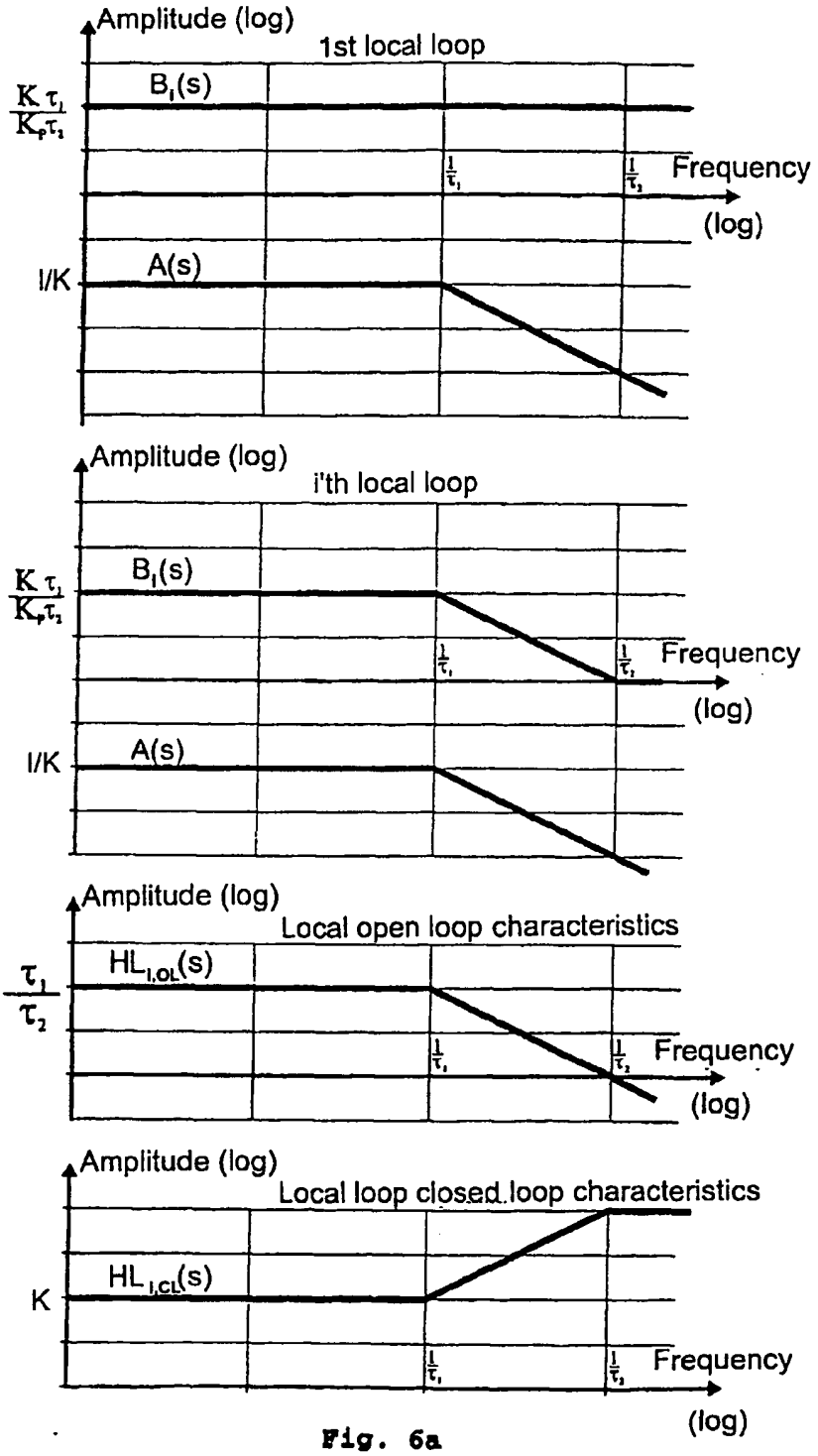
Amplitude (log)
1st local loop
$B_1(s)$
$\frac{K\tau_1}{K_p\tau_2}$
$\frac{1}{\tau_1}$
$\frac{1}{\tau_2}$
Frequency
(log)
I/K
A(s)
Amplitude (log)
i'th local loop
$B_i(s)$
$\frac{K\tau_i}{K_p\tau_2}$
$\frac{1}{\tau_i}$
$\frac{1}{\tau_2}$
Frequency
(log)
I/K
A(s)
Amplitude (log)
Local open loop characteristics
$HL_{i,OL}(s)$
$\frac{\tau_i}{\tau_2}$
$\frac{1}{\tau_i}$
$\frac{1}{\tau_2}$
Frequency
(log)
Amplitude (log)
Local loop closed loop characteristics
$HL_{i,CL}(s)$
K
$\frac{1}{\tau_i}$
$\frac{1}{\tau_2}$
Frequency
(log)

Fig. 6a

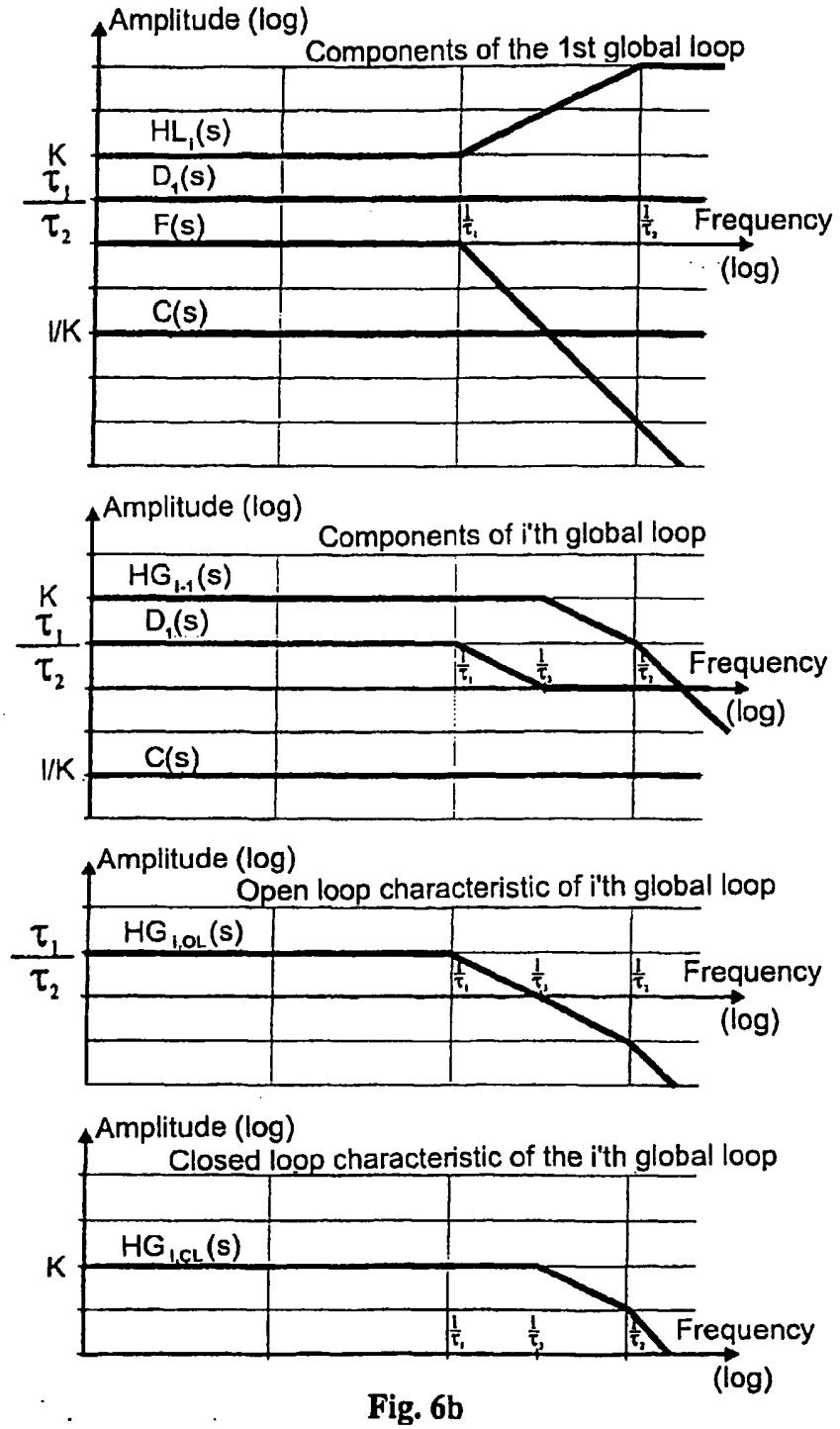
Amplitude (log)
Components of the 1st global loop
HL1(s)
K
τ1
D1(s)
τ2
F(s)
1/τ1
1/τ2
Frequency
(log)
C(s)
1/K
Amplitude (log)
Components of i'th global loop
HGi-1(s)
K
τ1
D1(s)
τ2
1/τ1
1/τi
1/τ2
Frequency
(log)
C(s)
1/K
Amplitude (log)
Open loop characteristic of i'th global loop
τ1
HGi,OL(s)
τ2
1/τ1
1/τi
1/τ2
Frequency
(log)
Amplitude (log)
Closed loop characteristic of the i'th global loop
K
HGi,CL(s)
1/τ1
1/τi
1/τ2
Frequency
(log)

Fig. 6b

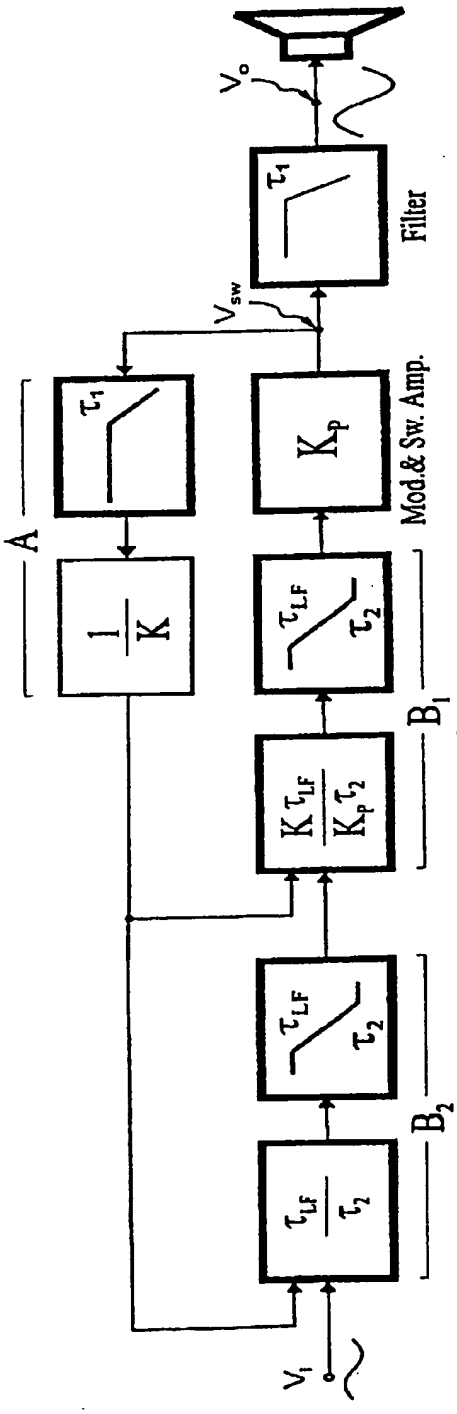
V_o
τ_1
Filter
V_{sw}
τ_1
K_p
Mod.& Sw. Amp.
A
$\frac{1}{K}$
τ_{LF} τ_2
B_1
$\frac{K\tau_{LF}}{K_p\tau_2}$
τ_{LF} τ_2
B_2
$\frac{\tau_{LF}}{\tau_2}$
V_i

Fig. 7

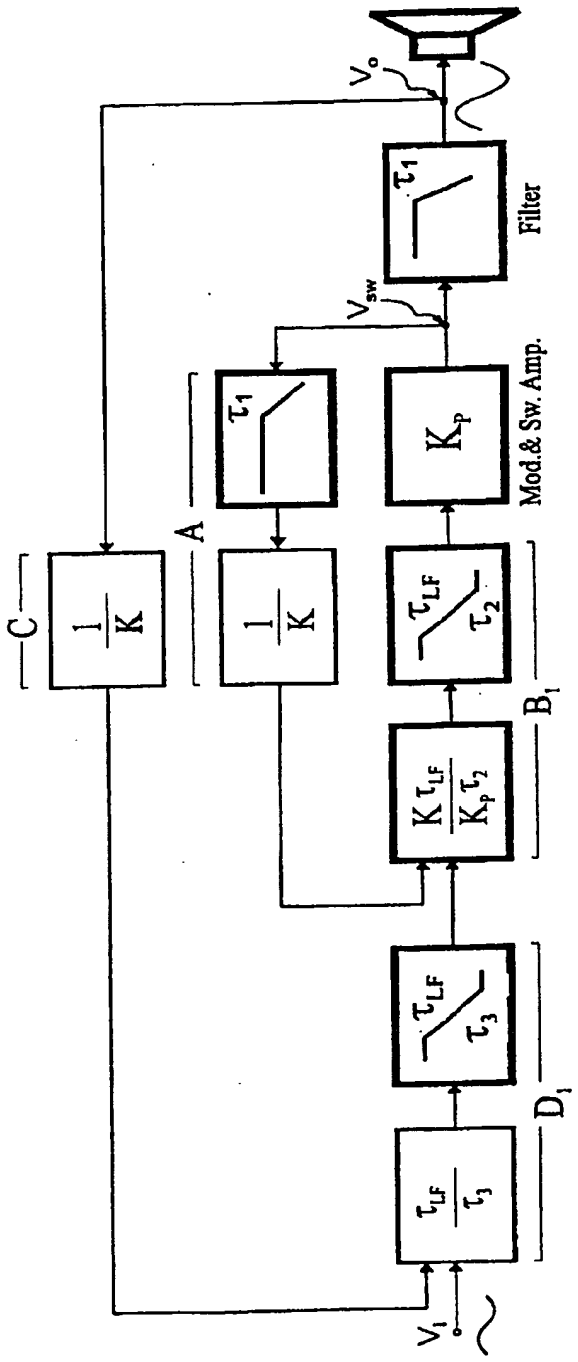
V_o
τ_1
Filter
V_{sw}
τ_1
K_p
Mod.& Sw. Amp.
A
C
$\frac{1}{K}$
$\frac{1}{K}$
τ_{LF}
τ_2
B_1
$\frac{K\tau_{LF}}{K_p\tau_2}$
τ_{LF}
τ_3
D_1
$\frac{\tau_{LF}}{\tau_3}$
V_i

Fig. 8

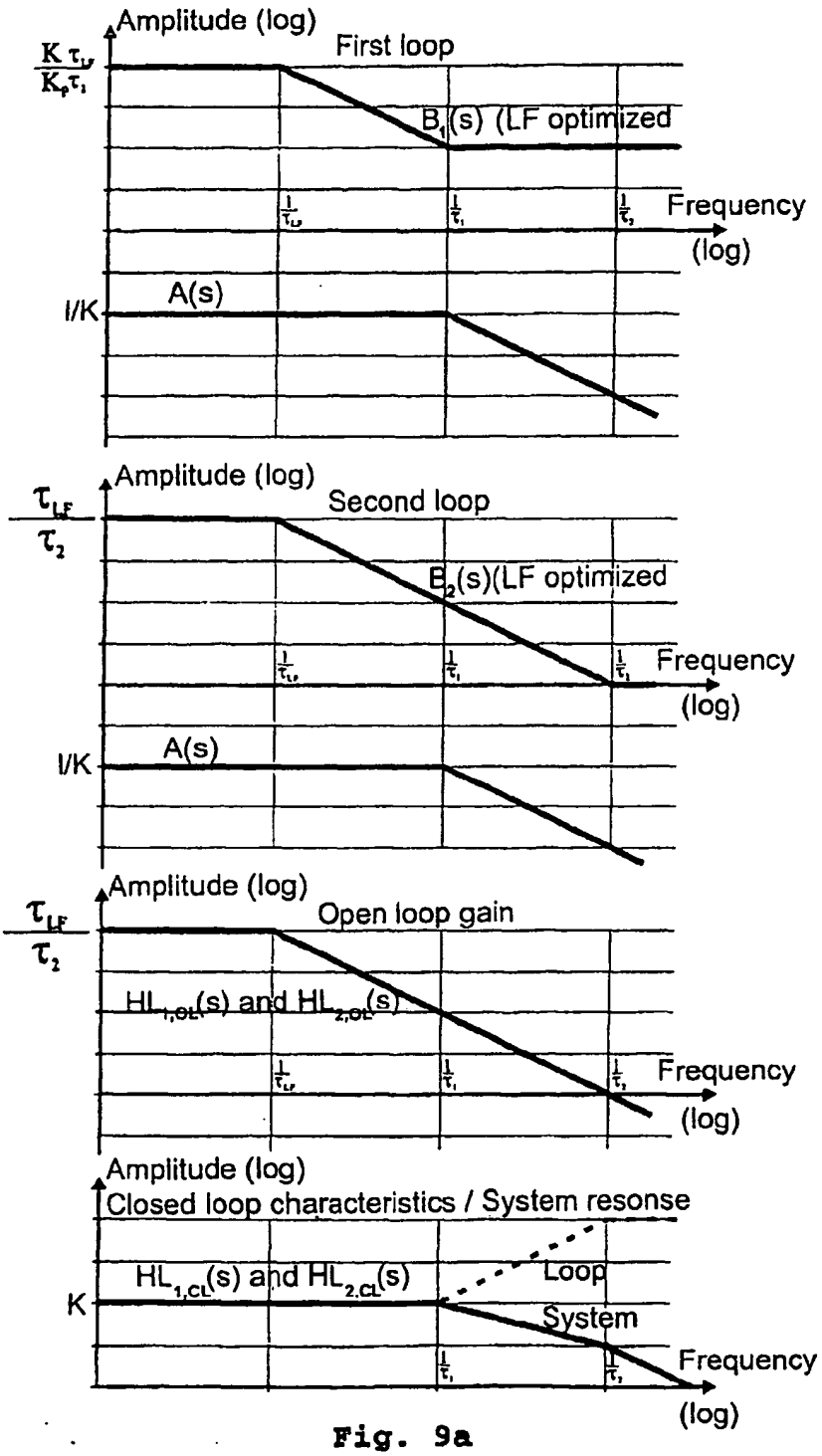
Amplitude (log)
First loop
B1(s) (LF optimized
Frequency
(log)
A(s)
I/K
Amplitude (log)
Second loop
B2(s)(LF optimized
Frequency
(log)
A(s)
I/K
Amplitude (log)
Open loop gain
HL1,OL(s) and HL2,OL(s)
Frequency
(log)
Amplitude (log)
Closed loop characteristics / System resonse
HL1,CL(s) and HL2,CL(s)
Loop
System
K
Frequency
(log)

Fig. 9a

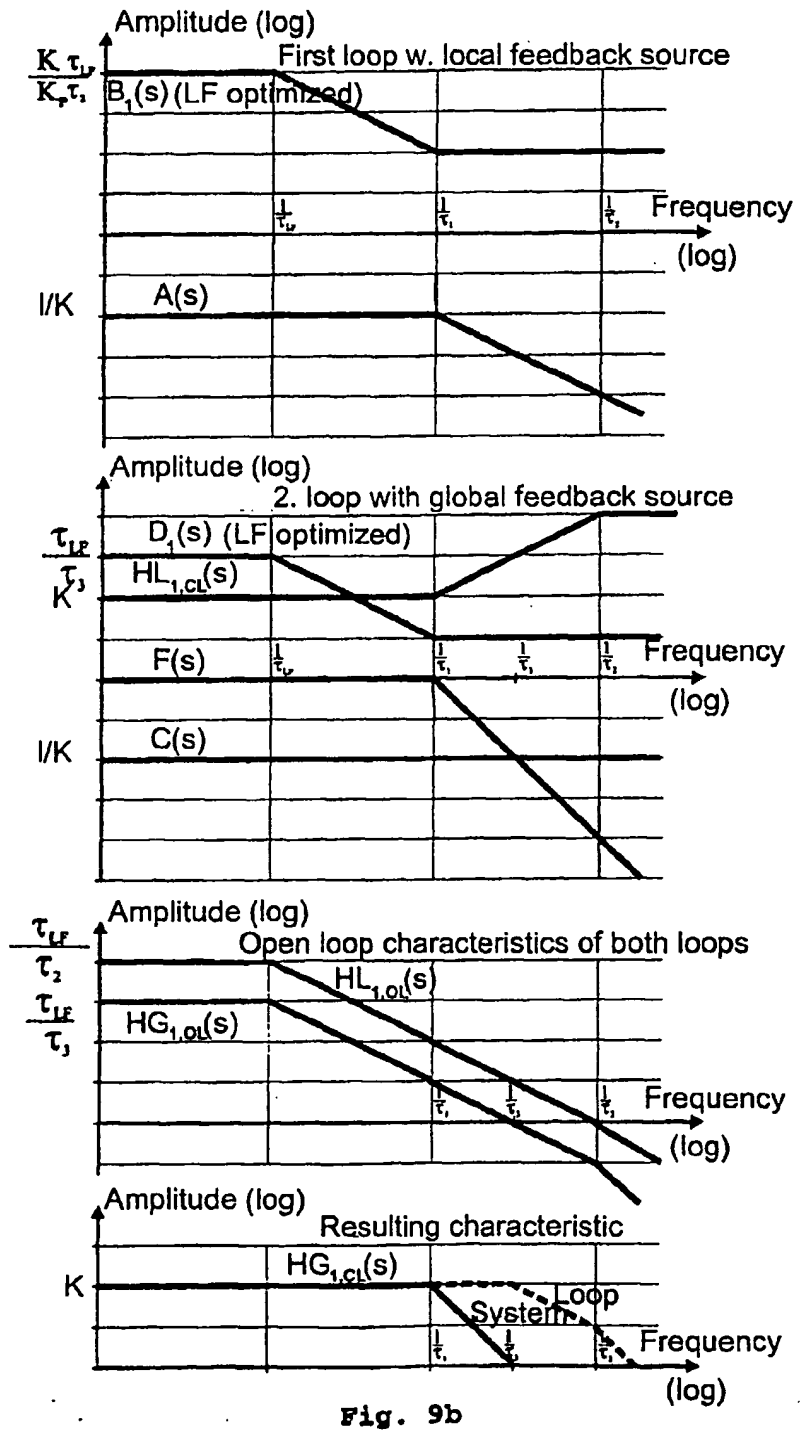
Amplitude (log)
First loop w. local feedback source
B1(s) (LF optimized)
Frequency
(log)
A(s)
Amplitude (log)
2. loop with global feedback source
D1(s) (LF optimized)
HL1,CL(s)
F(s)
Frequency
(log)
C(s)
Amplitude (log)
Open loop characteristics of both loops
HL1,OL(s)
HG1,OL(s)
Frequency
(log)
Amplitude (log)
Resulting characteristic
HG1,CL(s)
Loop
System
Frequency
(log)

Fig. 9b

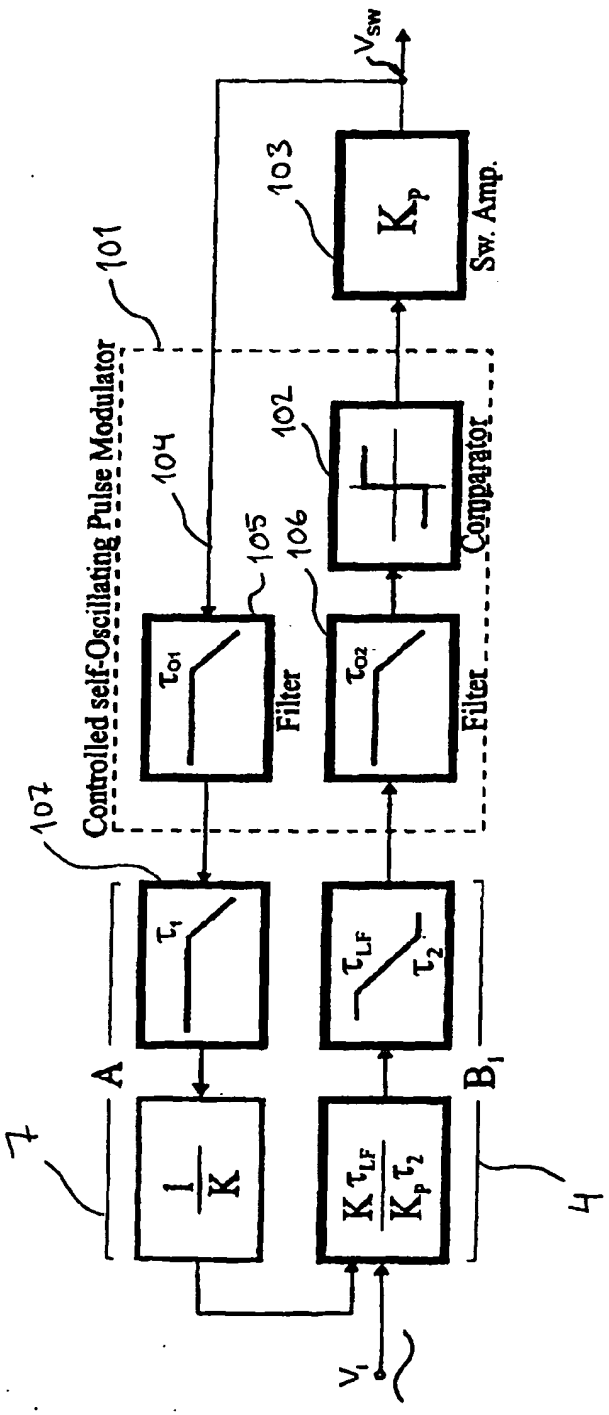
V_{sw}
103
K_p
Sw. Amp.
101
Controlled self-Oscillating Pulse Modulator
102
Comparator
104
105
106
τ_{o1}
Filter
τ_{o2}
Filter
107
τ_1
τ_{LF}
τ_2
A
B_1
7
$\frac{1}{K}$
$\frac{K\tau_{LF}}{K_p\tau_2}$
4
V_1

Fig. 10

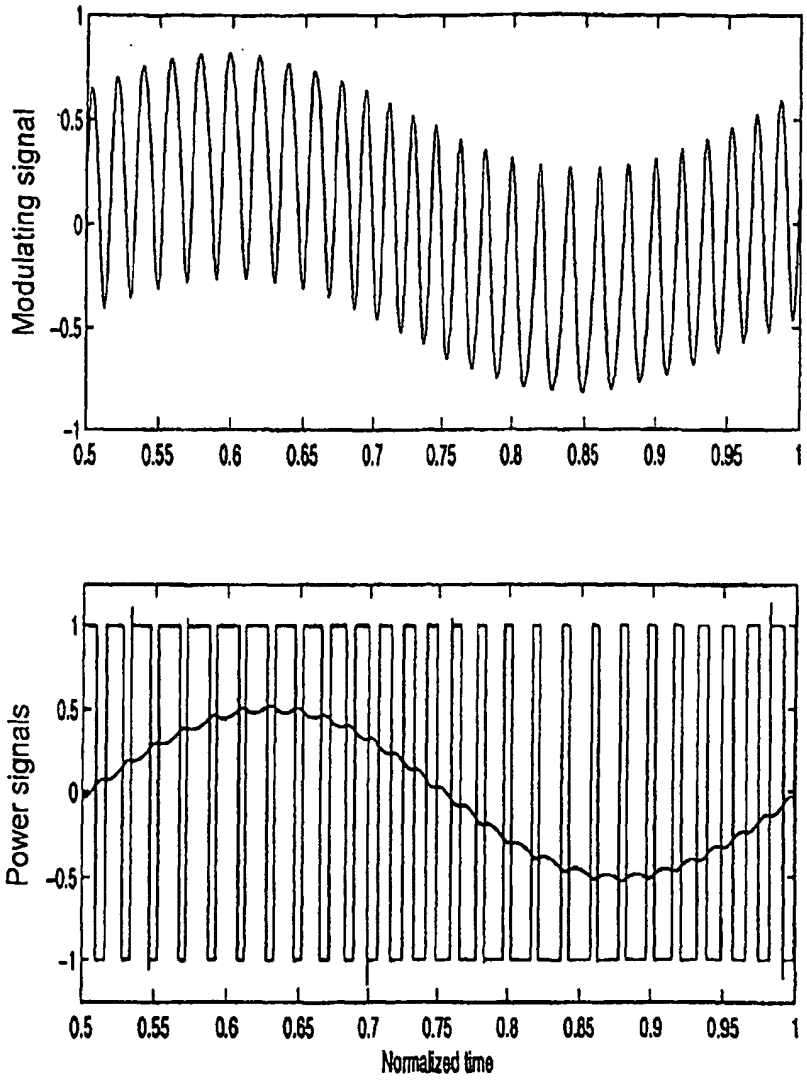
Modulating signal
1
0.5
0
-0.5
-1
0.5
0.55
0.6
0.65
0.7
0.75
0.8
0.85
0.9
0.95
1
Power signals
1
0.5
0
-0.5
-1
0.5
0.55
0.6
0.65
0.7
0.75
0.8
0.85
0.9
0.95
1
Normalized time

Fig. 11

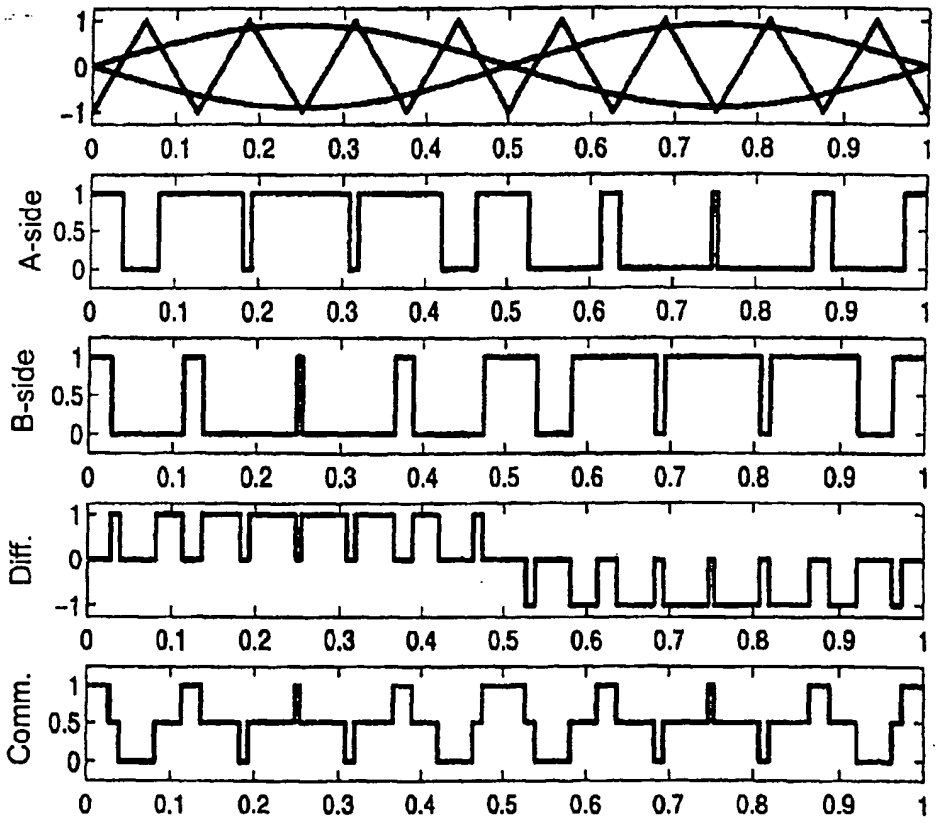

Fig. 12

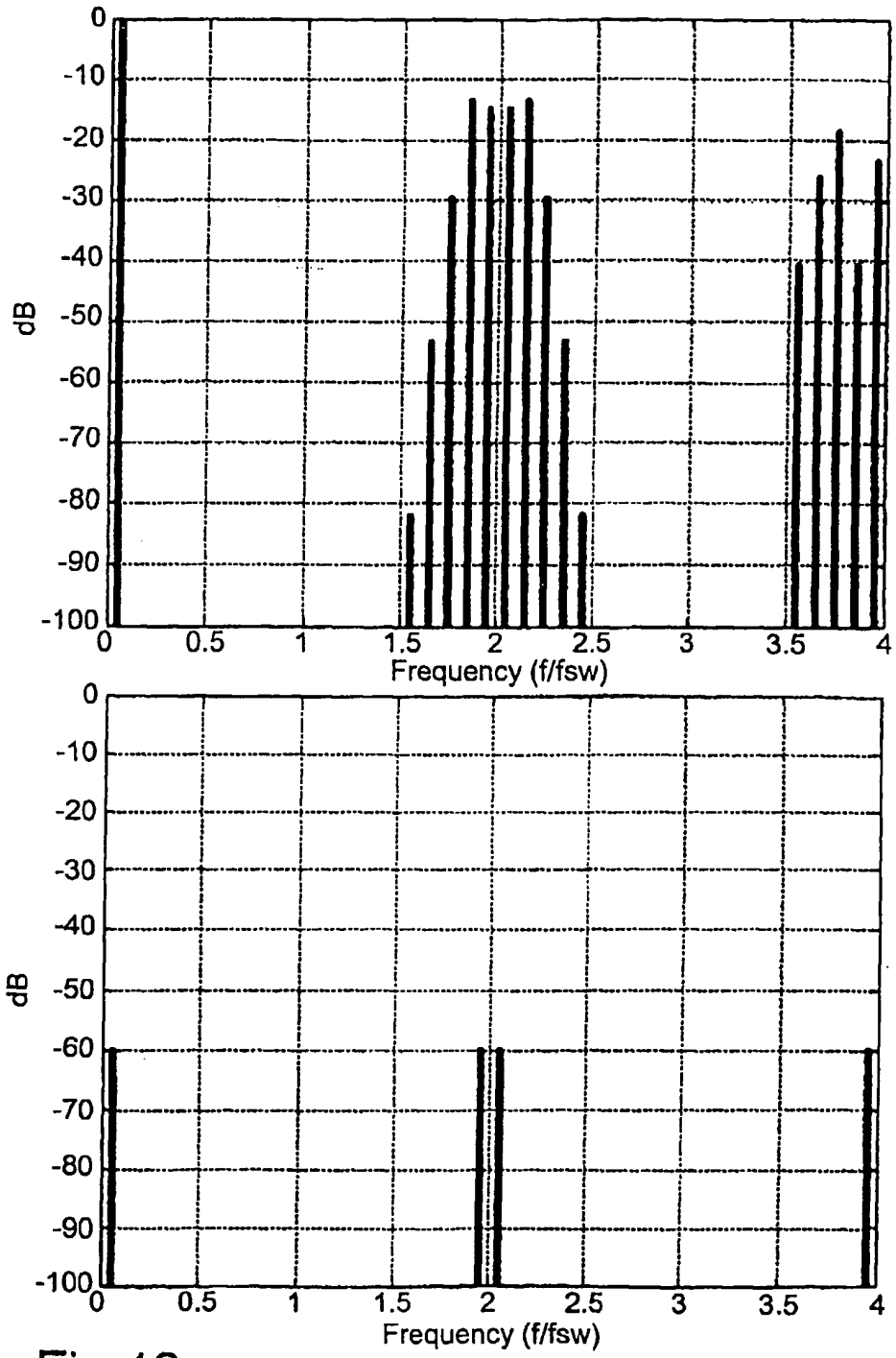
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
dB
0
0.5
1
1.5
2
2.5
3
3.5
4
Frequency (f/fsw)
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
dB
0
0.5
1
1.5
2
2.5
3
3.5
4
Frequency (f/fsw)

Fig.13

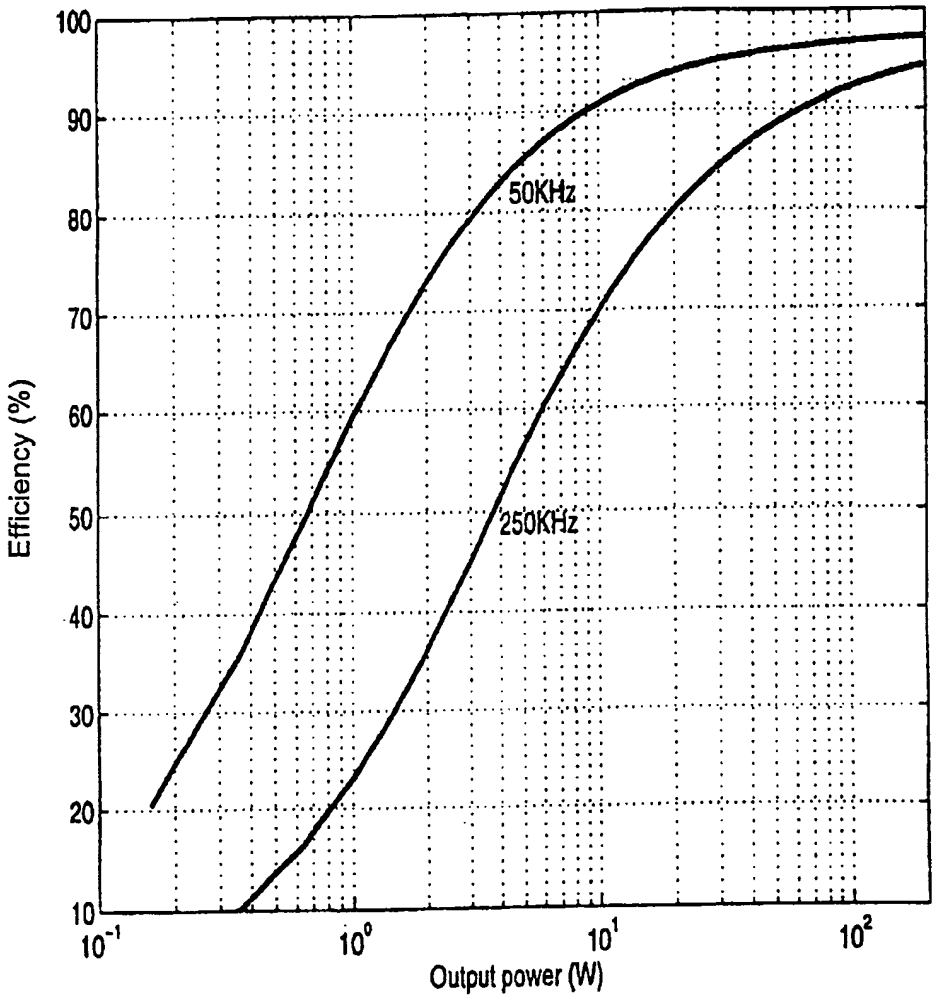
100
90
80
70
60
50
40
30
20
10
Efficiency (%)
50KHz
250KHz
10^{-1}
10^{0}
10^{1}
10^{2}
Output power (W)

Fig. 14a

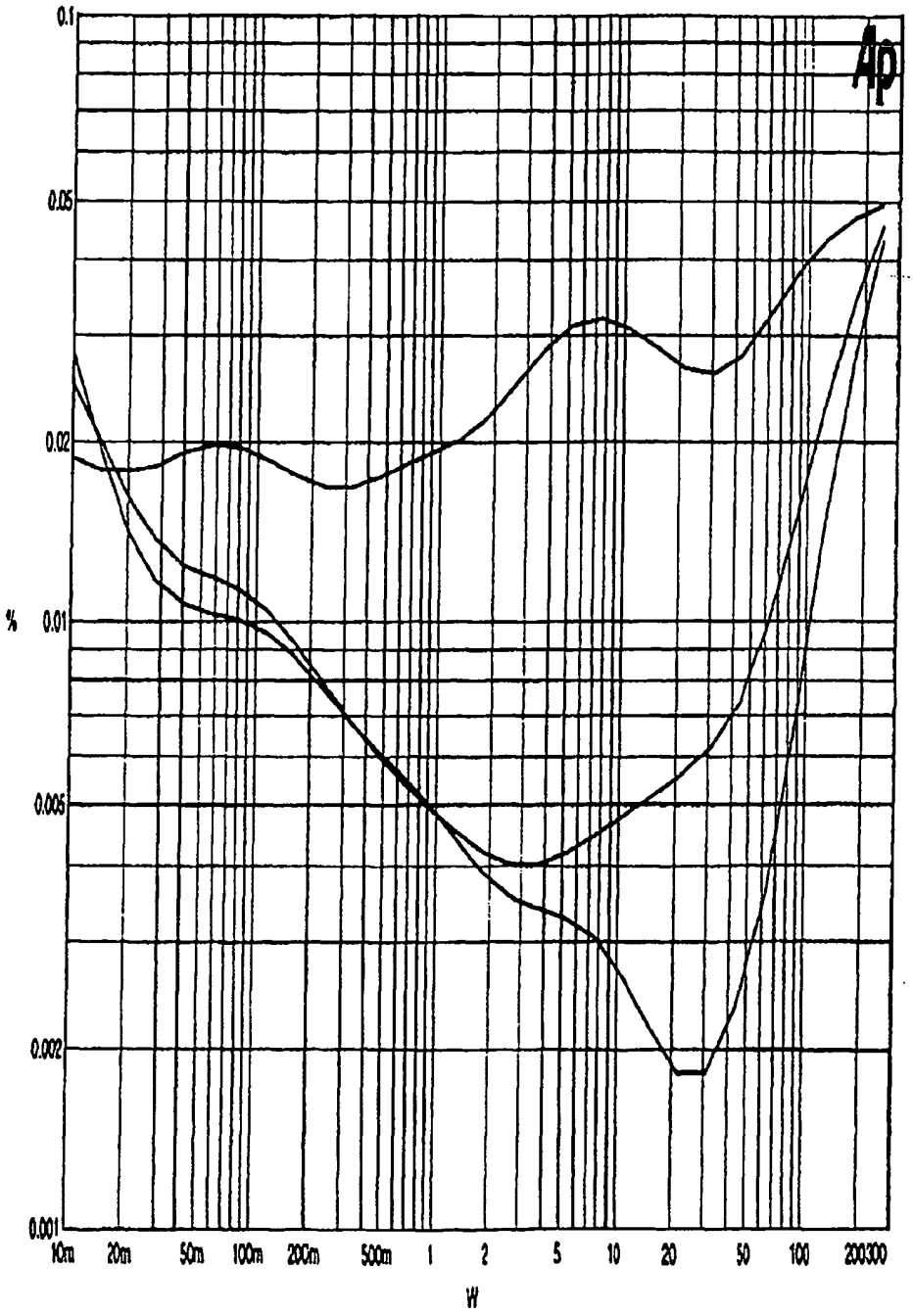
Ap
0.1
0.05
0.02
0.01
0.005
0.002
0.001
%
10m
20m
50m
100m
200m
500m
1
2
5
10
20
50
100
200300
W

Fig. 14b

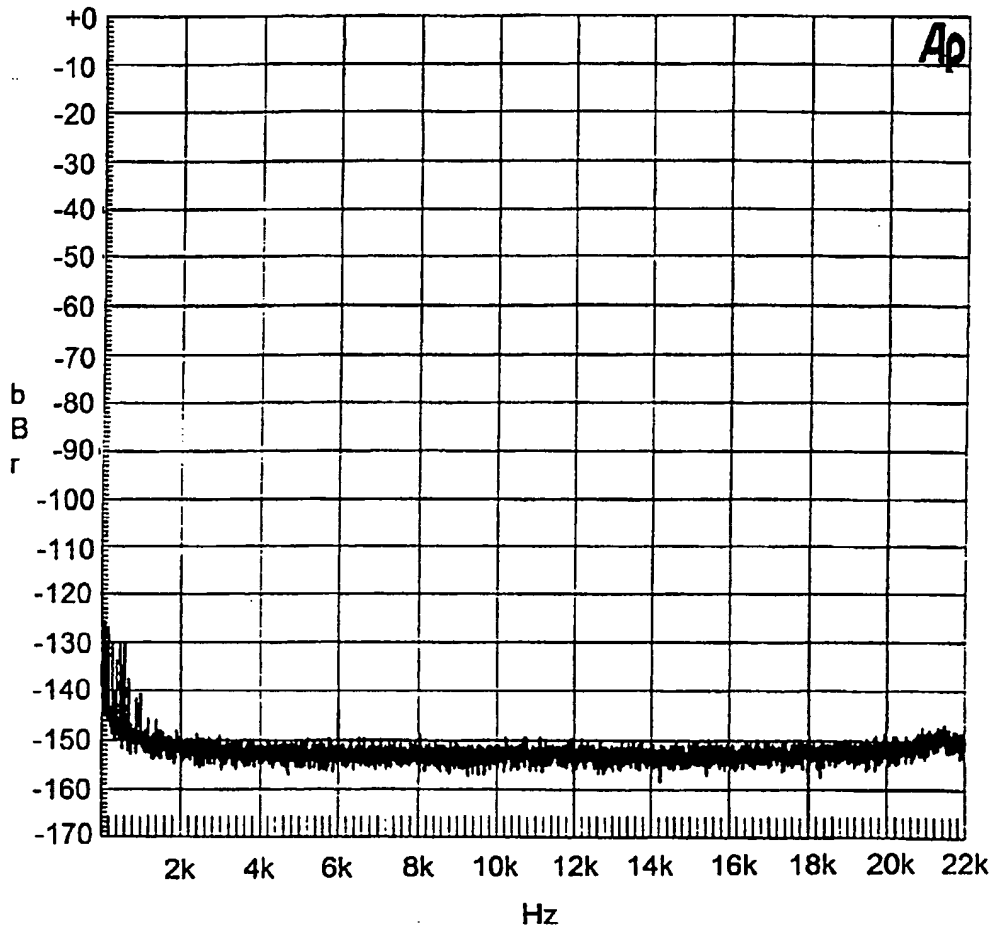
Ap
+0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
-130
-140
-150
-160
-170
b
B
r
2k
4k
6k
8k
10k
12k
14k
16k
18k
20k
22k
Hz

Fig. 14c

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 03 01 3623

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	PATENT ABSTRACTS OF JAPAN vol. 005, no. 095 (E-062), 20 June 1981 (1981-06-20) & JP 56 039606 A (MATSUSHITA ELECTRIC IND CO LTD), 15 April 1981 (1981-04-15) * abstract; figures 1-8 * ---	1-4,8, 10,11	H03F3/217
A	JEONG J H ET AL: "A CLASS D SWITCHING POWER AMPLIFIER WITH HIGH EFFICIENCY AND WIDE BANDWIDTH BY DUAL FEEDBACK LOOPS" INTERNATIONAL CONFERENCE ON CONSUMER ELECTRONICS - DIGEST OF TECHNICALPAPERS. ROSEMONT, JUNE 7 - 9 1995, NEW YORK, IEEE, US, vol. CONF. 14, 7 June 1995 (1995-06-07), pages 428-429, XP000547882 ISBN: 0-7803-2141-3 * the whole document * -----	1-11	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7) H03F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	22 October 2003	Agerbaek, T

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22-10-2003

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 56039606 A	15-04-1981	JP 1355422 C	24-12-1986
		JP 61021007 B	24-05-1986

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